

**Amendment and Response**

Applicant: Michael Bauer et al.

Serial No.: 10/789,033

Filed: February 27, 2004

Docket No.: I431.103.101/FIN 423 US

Title: ELECTRONIC COMPONENT AND SEMICONDUCTOR WAFER, AND METHOD FOR PRODUCING THE SAME

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The following remarks are made in response to the Non-Final Office Action mailed June 30, 2006. Claims 4-15 were rejected. With this Response, claim 15 is cancelled, claims 4-6 have been amended, and 18-20 were added. Claims 4-14 and 18-20 remain pending in the application and are presented for reconsideration and allowance.

**In the Drawings**

The Examiner objected to the drawings under 37 C.F.R. 1.83(a). The drawings must show every feature of the invention specified in the claims. Claim 13 has now been amended to clarify that it is a contact pad, which is illustrated in the Figures, and not a contact path. As such, Applicants now believe the drawings are in condition for allowance.

**Claim Rejections under 35 U.S.C. § 102**

The Examiner rejected claim 4 under 35 U.S.C. § 102(b) as being anticipated by the Nelson et al. U.S. Patent No. 4,930,216. The Examiner rejected claim 5 under 35 U.S.C. § 102(b) as being anticipated by the Nakajima reference, Japanese Patent No. 2002-299372. Finally, the Examiner rejected claims 6-14 under 35 U.S.C. § 102(b) as being anticipated by the Nakajima reference, Japanese Patent No. 2002-299372.

With the present response, claims 4-6 have been amended to incorporate the limitations of claim 15. Furthermore, since dependant claims 7-14 depend from these claims, they also include these limitations. Consequently, the cited references do not anticipate these claims.

Therefore, Applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. § 102(b) rejection to claims 4-14, and request allowance of these claims.

**Claim Rejections under 35 U.S.C. § 103**

The Examiner rejected claims 13 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Nakajima reference in view of the Fukatsu et al. U.S. Patent No. 6,528,870.

As indicated above, applicant amended claims 4-6 to include limitations from claim 15. In addition, claims 18-20 have been added with similar features. These additional claims are

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supported at least by the embodiment illustrated in Figures 9 and 10 of the application, as well as the embodiment described on page 5, lines 20 to 29, page 7, line 28 to page 8, line 7 and page 132, lines 5-27.

As such, in this embodiment, the semiconductor chips are memory components. The semiconductor chips have edge contacts which enable them to be mounted on a circuit substrate so that the rear side of the semiconductor chips is approximately perpendicular to the top surface of the circuit substrate. The circuit substrate is provided with bus lines which enable a plurality of the memory chips to be mounted on the circuit substrate in parallel. This enables a high packing density due to the size of the memory components, which is essentially the size of the semiconductor chip, and the tight packing enabled by the vertical stacking arrangement on the common bus lines. None of the art of record teaches or suggests this embodiment.

The Examiner cites the Nakajima reference connection with claim 14, specifically Figures 2 and 4. All of the currently pending claims, however, are now clarified such that the rear side is arranged approximately perpendicular to the top side of the circuit substrate. The Nakajima and art of record fail to teach or suggest this relationship.

Regarding claim 15, the Examiner cites the Fukatsu patent. The Fukatsu patent teaches electronic components comprising a semiconductor chip and a substrate. The edge contacts are arranged in the substrate rather than in the semiconductor chips itself. Furthermore, the Fukatsu patent fails to teach a stack of semiconductor chips in which the rear side of the semiconductor chips is approximately perpendicular to the insulated substrate on which it is mounted. In the stacks taught by the Fukatsu, the rear surface of the semiconductor chips is arranged parallel to the top side of the circuit substrate.

Consequently, the arrangement of a plurality of memory components and insulated circuit substrate according to the pending claims are not obvious from the art of record.

Therefore, Applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection to claims 13 and 15, and request allowance of all pending claims.

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**CONCLUSION**

In view of the above, Applicant respectfully submits that pending claims 4-14 and 18-20 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 4-14 and 18-20 are respectfully requested.

Applicants hereby authorize the Commissioner for Patents to charge Deposit Account No. 50-0471 in the amount of 200.00 to cover the fees as set forth under 37 C.F.R. 1.16(h)(i).

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

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Any inquiry regarding this Amendment and Response should be directed to Paul Kempf at Telephone No. (612) 767-2502, Facsimile No. (612) 573-2001. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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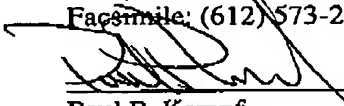
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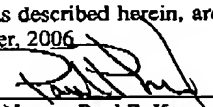
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**CERTIFICATE UNDER 37 C.F.R. 1.8:**

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via facsimile to Facsimile No. (571) 273-8300 on this 2<sup>nd</sup> day of October, 2006.

By:   
Name: Paul P. Kempf